Claims

[1] 1. A gallium nitride-based III-V group compound semiconductor device comprising:
a gallium nitride-based semiconductor layer; and
an ohmic electrode layer formed on the gallium nitride-based semiconductor layer,
wherein the ohmic electrode layer comprises a contact metal layer, a reflective metal layer, and a diffusion barrier layer.

[2] 2. The semiconductor device according to claim 1, wherein the ohmic electrode layer further comprises at least one bonding metal layer.

[3] 3. The semiconductor device according to claim 2, wherein the ohmic electrode layer is formed by sequentially laminating the contact metal layer, the reflective metal layer, the diffusion barrier layer, and the bonding metal layer.

[4] 4. The semiconductor according to any one of claims 1 to 3, wherein the contact metal layer comprises at least one of Ni, Ir, Pt, Pd, Au, Ti, Ru, W, Ta, V, Co, Os, Re, and Rh.

[5] 5. The semiconductor according to any one of claims 1 to 3, wherein the reflective metal layer comprises at least one of Al and Ag.

[6] 6. The semiconductor according to any one of claims 1 to 3, wherein the diffusion barrier layer comprises at least one of Ru, Ir, Re, Rh, Os, V, Ta, W, ITO (Indium Tin Oxide), IZO (Indium Zinc oxide), RuO_2, VO_2, MgO, IrO_2, ReO_2, RhO_2, OsO_2, Ta_2O_3, and WO_2.

[7] 7. The semiconductor according to claim 2 or 3, wherein the bonding metal layer comprises first and second bonding metal layers, said first bonding metal layer comprising at least one of Ni, Cr, Ti, Pd, Ru, Ir, Rh, Re, Os, V, and Ta, said second bonding metal layer comprising at least one of Au, Pd, and Pt.

[8] 8. A method of manufacturing a gallium nitride-based III-V group compound semiconductor device, comprising steps of:
forming a gallium nitride-based semiconductor layer having a PN contact structure on a substrate; and
forming an ohmic electrode layer on the semiconductor layer,
wherein the ohmic electrode layer comprises a contact metal layer, a reflective metal layer, and a diffusion barrier layer.

[9] 9. The method of according to claim 8, wherein the step of forming the ohmic

electrode layer comprises steps of:

sequentially laminating the contact metal layer, the reflective metal layer, and the diffusion barrier layer on the semiconductor layer;

performing a thermal treatment process; and

forming a bonding metal layer on the diffusion barrier layer.

[10] 10. The method of according to claim 8, wherein the step of forming the ohmic electrode layer comprises steps of:

sequentially laminating the contact metal layer, the reflective metal layer, the diffusion barrier layer and bonding metal layer on the semiconductor layer; and

performing a thermal treatment process.

[11] 11. The method of according to any one of claims 8 to 10, wherein the thermal treatment process is a rapid thermal annealing process performed under an atmosphere of 5 to 100% oxygen at a temperature of 100 to 700 °C for 10 to 100 seconds.